

CLAIMS

What is claimed is:

1 1. A method for synchronizing clocks in a network, the method
2 comprising the steps of:

3 receiving a first timestamp and a second timestamp each
4 indicating a respective time instance as determined by a first
5 clock signal within the network;

6 measuring a first time interval between the first timestamp
7 and the second timestamp;

8 generating a difference signal representing a difference
9 between the first time interval and a second time interval; and

10 generating a second clock signal based upon the difference
11 signal such that the second clock signal is synchronized with
12 the first clock signal.

1 2. The method as defined in claim 1, further comprising the
2 step of:

3 generating a third timestamp and a fourth timestamp each
4 indicating a respective time instance as determined by the
5 second clock signal.

1 3. The method as defined in claim 2, further comprising the
2 step of:

3 measuring the second time interval between the third
4 timestamp and the fourth timestamp.

1 4. The method as defined in claim 3, wherein the first
2 timestamp and the third timestamp are each generated at a first
3 discrete time instant, and the second timestamp and the fourth
4 timestamp are each generated at a second discrete time instant.

1 5. The method as defined in claim 1, further comprising the
2 step of:

3 initializing the difference signal prior to receiving the
4 first timestamp and the second timestamp.

1 6. The method as defined in claim 1, further comprising the
2 step of:

3 filtering the difference signal such that the second clock
4 signal is synchronized with the first clock signal based upon a
5 filtered difference signal.

1 7. The method as defined in claim 6, further comprising the
2 step of:

3 initializing the filtered difference signal prior to
4 receiving the first timestamp and the second timestamp.

1 8. The method as defined in claim 1, wherein the step of
2 generating the second clock signal comprises the step of:
3 controlling the period of a digitally controlled oscillator
4 based upon the difference signal.

1 9. The method as defined in claim 1, wherein the step of
2 generating the second clock signal comprises the step of:
3 converting the difference signal from a digital difference
4 signal value into analog difference signal value; and
5 controlling the period of a voltage controlled oscillator
6 based upon the analog difference signal value.

1 10. A computer signal embodied in a carrier wave readable by a
2 computing system and encoding a computer program of instructions
3 for executing a computer process performing the method recited
4 in claim 1.

1 11. An apparatus for synchronizing clocks in a network, the
2 apparatus comprising:
3 a receiver for receiving a first timestamp and a second

4 timestamp each indicating a respective time instance as
5 determined by a first clock signal within the network; and
6 a phase-locked loop associated with the receiver, the
7 phase-locked loop comprising:

8 a first differencing element for measuring a first
9 time interval between the first timestamp and the second
10 timestamp;

11 a second differencing element for generating a
12 difference signal representing a difference between the first
13 time interval and a second time interval; and

14 a variable oscillator for generating a second clock
15 signal based upon the difference signal such that the second
16 clock signal is synchronized with the first clock signal.

17 12. The apparatus as defined in claim 11, further comprising:

18 a pulse counter for generating a third timestamp and a
19 fourth timestamp each indicating a respective time instance as
20 determined by the second clock signal.

21 13. The apparatus as defined in claim 12, further comprising:

22 a third differencing element for measuring the second time
23 interval between the third timestamp and the fourth timestamp.

1 14. The apparatus as defined in claim 13, wherein the first
2 timestamp and the third timestamp are each generated at a first
3 discrete time instant, and the second timestamp and the fourth
4 timestamp are each generated at a second discrete time instant.

1 15. The apparatus as defined in claim 11, wherein the second
2 differencing element initializes the difference signal prior to
3 receiving the first timestamp and the second timestamp.

16. The apparatus as defined in claim 11, further comprising:
a loop filter for filtering the difference signal such that
the second clock signal is synchronized with the first clock
signal based upon a filtered difference signal.

17. The apparatus as defined in claim 16, wherein the loop
2 filter initializes the filtered difference signal prior to
3 receiving the first timestamp and the second timestamp.

1 18. The apparatus as defined in claim 11, wherein the variable
2 oscillator is a digitally controlled oscillator the period of
3 which is controlled based upon the difference signal.

1 19. The apparatus as defined in claim 11, further comprising:

2 a digital-to-analog converter for converting the difference
3 signal from a digital difference signal value into analog
4 difference signal value, and wherein the variable oscillator is
5 a voltage controlled oscillator the period of which is
6 controlled based upon the analog difference signal value.

1 20. An article of manufacture for synchronizing clocks in a
2 network, the article of manufacture comprising:

3 at least one processor readable carrier; and
4 instructions carried on the at least one carrier;
5 wherein the instructions are configured to be readable from
6 the at least one carrier by at least one processor and thereby
7 cause the at least one processor to operate so as to:

8 receive a first timestamp and a second timestamp each
9 indicating a respective time instance as determined by a first
10 clock signal within the network;

11 measure a first time interval between the first timestamp
12 and the second timestamp;

13 generate a difference signal representing a difference
14 between the first time interval and a second time interval; and

15 generate a second clock signal based upon the difference
16 signal such that the second clock signal is synchronized with
17 the first clock signal.